DDR Termination Regulator

FEATURES

- AVIN Input Voltage Range: 2.375V to 5.5V
- PVIN Input Voltage Range: 1.1V to AVIN
- 2A Source and Sink Current Capability
- Support DDR / DDRII / DDRIII/ Low Power DDRIII / DDRIV Requirements
- Low Output Voltage Offset, ±20mV
- High Accuracy Output Voltage at Full-Load
- Stable with 22μF Ceramic Output Capacitor
- Low External Component Count
- No External Resistor Required
- Built in Soft Start, UVLO and OCP Protection
- Thermal Shutdown Protection
- SOP-8 Exposed Pad Package
- RoHS Compliant and Green Package

APPLICATIONS

- Desktop PCs, Notebooks and Workstations
- Graphic Cards
- Set Top Boxes, Digital TVs, Printers
- DDR/II/III Termination Voltage Supply

DESCRIPTION

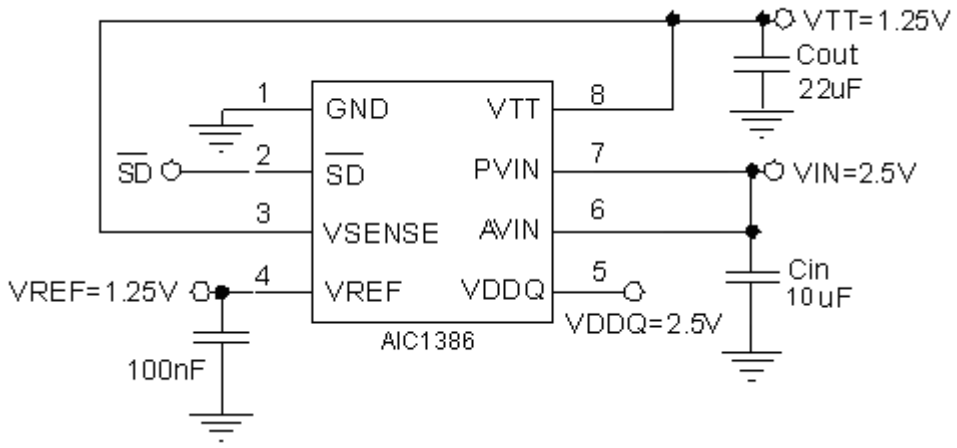
AIC1386 linear regulator is designed to achieve 2A source and sink current for termination of. DDR / DDRII / DDRIII while regulating an output voltage to within ±20mV. And it can deliver 1.5A continue current for termination of DDRIV.

AIC1386 converts voltage supplies range from 1.1V to 5.5V into an output voltage that adjusts by two external voltage divider resistors. It provides an excellent voltage source for active termination schemes of high-speed transmission lines as those seen in double data rate (DDR) memory system, and it meets the JEDEC SSTL-2 and SSTL-18 or other specific interfaces such as HSTL, SCSI-1 and SCSI-3 specifications for termination of DDR-SRAM.

Built-in current limiting in source and sink mode, on-chip thermal shutdown protection to against fault conditions.

The AIC1386 is available in the SOP-8 with exposed pad package

TYPICAL APPLICATION CIRCUIT



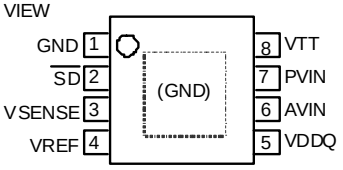
ORDERING INFORMATION

AIC1386XXXXX

- PACKING TYPE
  TR: TAPE & REEL
  TB: TUBE
- PACKAGING TYPE
  R8: SOP-8 Exposed Pad (Heat Sink)
- G: Green Package

PIN CONFIGURATION

SOP-8 Exposed Pad (Heat Sink)
TOP VIEW



Note:
The exposed pad must be connected with GND pin.

Example: AIC1386GR8TR

→ In Green SOP-8 Exposed Pad (Heat Sink)Package & Taping & Reel Packing

ABSOLUTE MAXIMUM RATINGS

PVIN, AVIN, VDDQ, $\overline{SD}$, VSENSE, VREF, VTT, to GND ..... -0.3V to 6V

Operating Temperature Range ..... -40°C ~ 85°C

Junction Temperature ..... 150°C

Storage Temperature Range ..... - 65°C ~ 150°C

Lead Temperature (Soldering. 10 sec) ..... 260°C

Thermal Resistance Junction to Ambient, $R\theta_{JA}$ SOP-8 Exposed Pad (Heat Sink)* ..... 60°C /W

Thermal Resistance Junction to Case, $R\theta_{JC}$ SOP-8 Exposed Pad (Heat Sink) * ..... 16°C /W

(Assume no Ambient Airflow)

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

*The package is place on a two layers PCB with 2 ounces copper and 2 square inch, connected by 8 vias.

ELECTRICAL CHARACTERISTICS

(AVIN=5V, PVIN=VDDQ=1.8V, VREF=0.5VDDQ, T_A=25°C, unless otherwise specified) (Note 1)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
Input Voltage Range		AVIN	2.375		5.5	V
		PVIN	1.1		AVIN	V
		VDDQ	1.1		PVIN	V
SUPPLY CURRENT						
AVIN Supply Current	AVIN=5V, I_{OUT} = 0A	I_{Q-AVIN}	0.3	1	2	mA
AVIN Standby Current	AVIN=5V, SDN= 0V, VREF> 0.39V	$I_{STBY-AVIN}$		60		µA
	AVIN=5V, SDN= 0V, VREF< 0.39V	$I_{REFUVLO-AVIN}$		30		µA
VDDQ Quiescent Current	AVIN=5V, SDN= 0V, VREF< 0.39V	I_{Q-VDDQ}		10		µA
PVIN Standby Current	AVIN=5V, SDN= 0V, VREF> 0.39V	$I_{STBY-PVIN}$		2	90	µA
	AVIN=5V, SDN= 0V, VREF< 0.39V	$I_{SD-PVIN}$		2	90	µA
VTT OUTPUT						
VTT Output Voltage	PVIN=VDDQ=2.5V	VTT		1.25		V
	PVIN=VDDQ=1.8V			0.9		
	PVIN=VDDQ=1.5V			0.75		
VTT Output Offset	I_{OUT} = 0A	Vos_VTT	-20		20	mV
VTT Load Regulation	I_{OUT} =0.1mA ~ +2A	ΔV_{LOR}	-20		20	mV
	I_{OUT} =0.1mA ~ -2A		-20		20	
VTT Current Limit	Source/Sink current	I_{LIM}	2.4	3		A
VTT Discharge Current	V_{REF}=0V, V_{OUT}=0.3V	I_{DSCHG}	12	17		mA
V_{SENSE} Input Current		I_{VSENSE}		13		nA
VREF OUTPUT						
VREF Output Voltage	PVIN=VDDQ=2.5V	VREF		1.25		V
	PVIN=VDDQ=1.8V			0.9		
	PVIN=VDDQ=1.5V			0.75		
VREF Output Voltage Tolerance to VDDQ/2	PVIN=VDDQ=2.5V, I_{VREF} = 10mA	V_{REFTOL}	-20		20	mV
	PVIN=VDDQ=1.8V, I_{VREF} = 10mA	V_{REFTOL}	-18		18	mV
	PVIN=VDDQ=1.5V, I_{VREF} = 10mA	V_{REFTOL}	-15		15	mV
LOGIC THRESHOLD						
Shutdown Threshold	Output ON	V_{IH}	1.6			V
	Output OFF	V_{IL}			0.3	
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_{SD}		160		°C
Thermal Shutdown Hysteresis				30		

Note1: Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: V_{OS} is the voltage measurement, which is defined as V_{TT} subtracted V_{REF}.

Note 3: Load regulation is measured at constant junction temperature, using pulse testing with a low ON time.

Note 4: Current limit is measured by pulse load.

TYPICAL PERFORMANCE CHARACTERESTECS

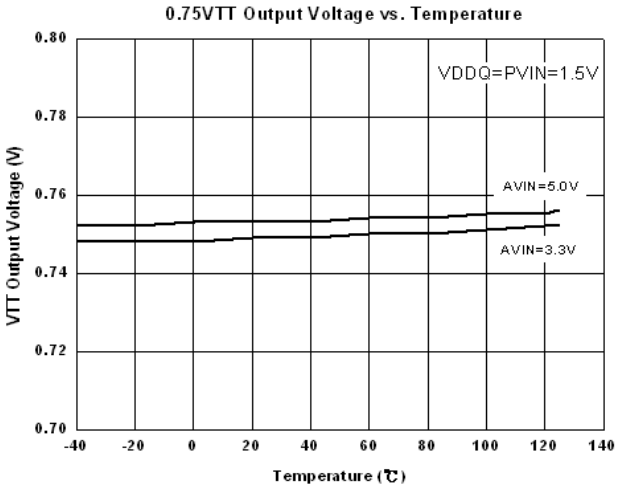


Fig.1 0.75VTT Output Voltage vs. Temperature

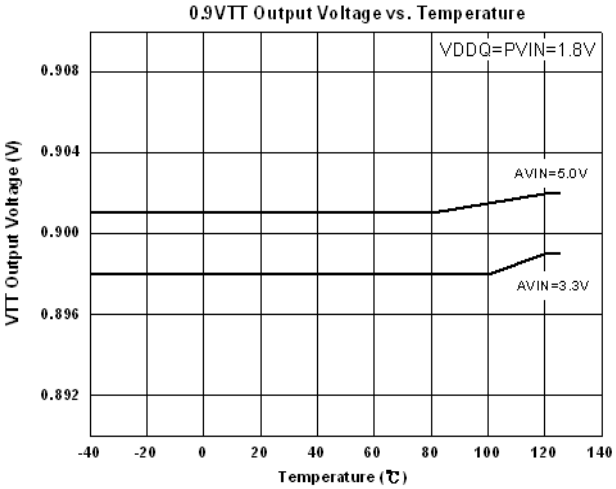


Fig.2 0.90VTT Output Voltage vs. Temperature

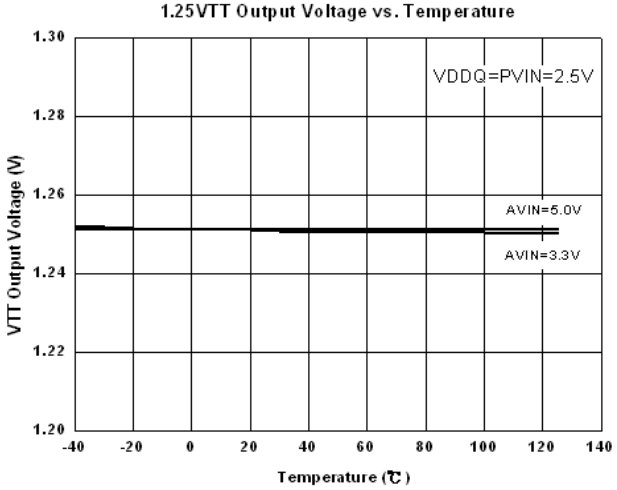


Fig.3 1.25VTT Output Voltage vs. Temperature

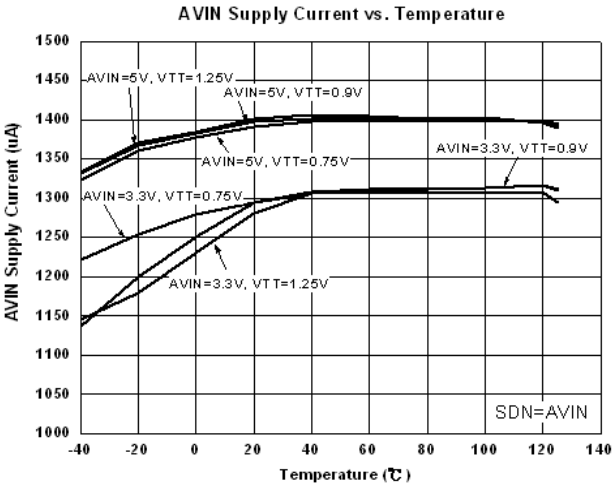


Fig.4 AVIN Supply Current vs. Temperature

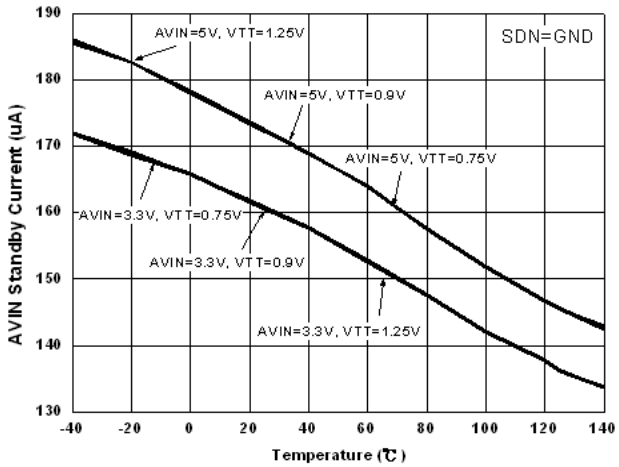


Fig.5 AVIN Standby Current vs. Temperature

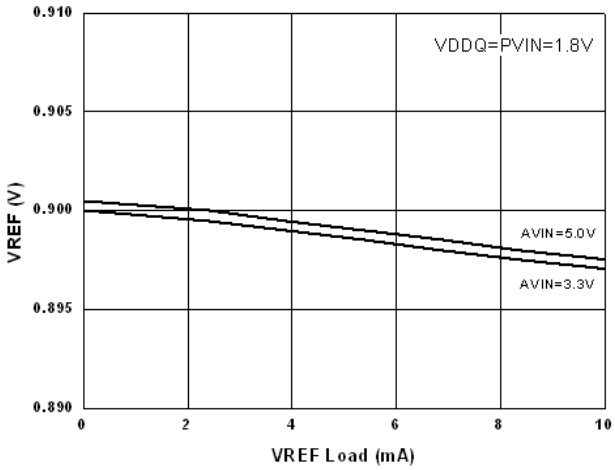


Fig.6 VREF Output Voltage vs. VREF Load Current

TYPICAL PERFORMANCE CHARACTERESTECS (Continued)

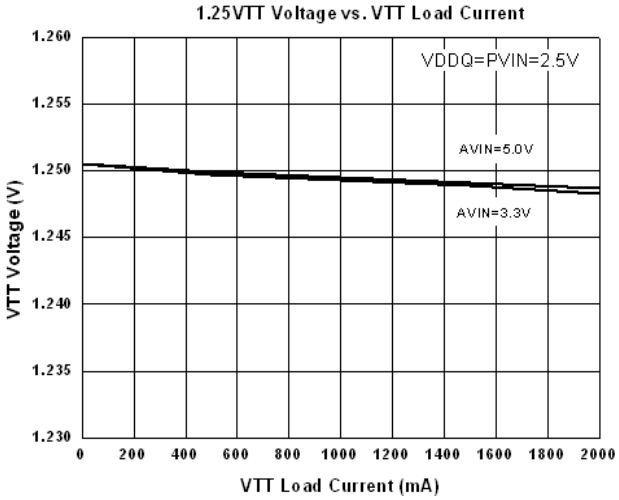


Fig.7 1.25VTT Voltage vs. VTT Load Current

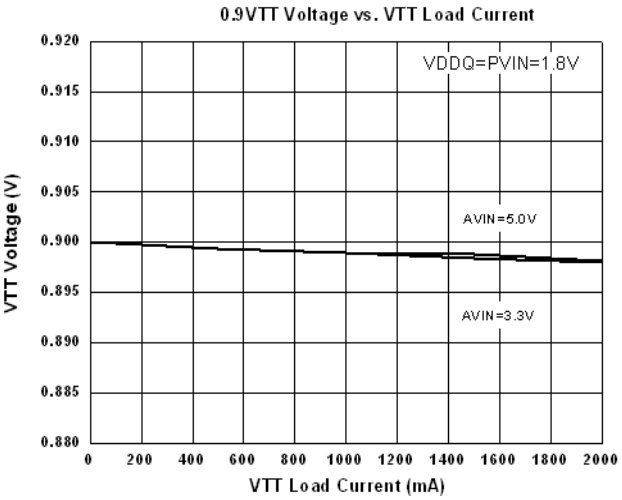


Fig.8 0.9VTT Voltage vs. VTT Load Current

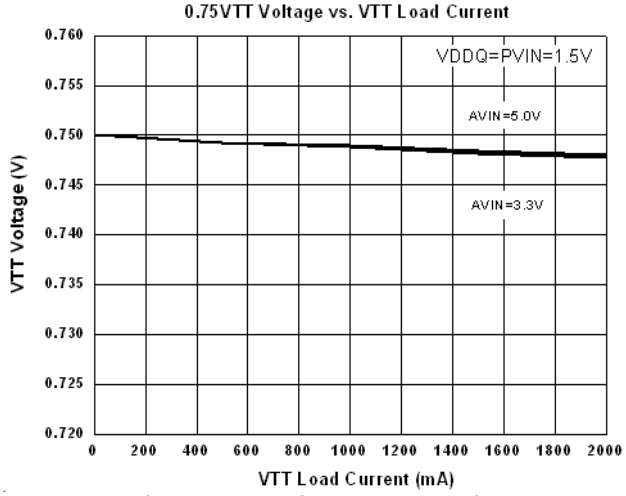


Fig.9 0.75VTT Voltage vs. VTT Load Current

TYPICAL PERFORMANCE CHARACTERESTECS (Continued)

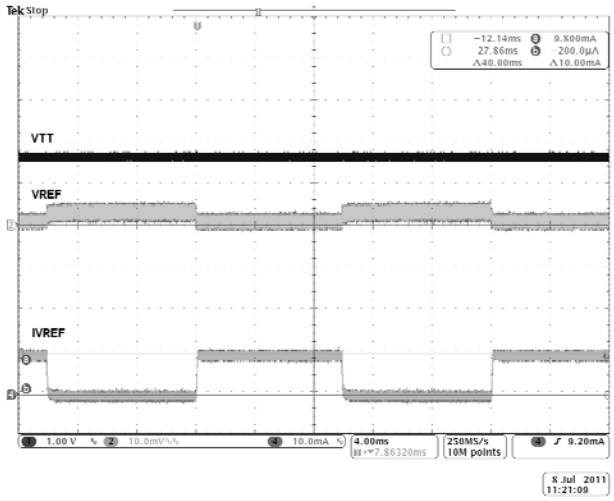


Fig.12 0.75VREF in 10mA Transient response

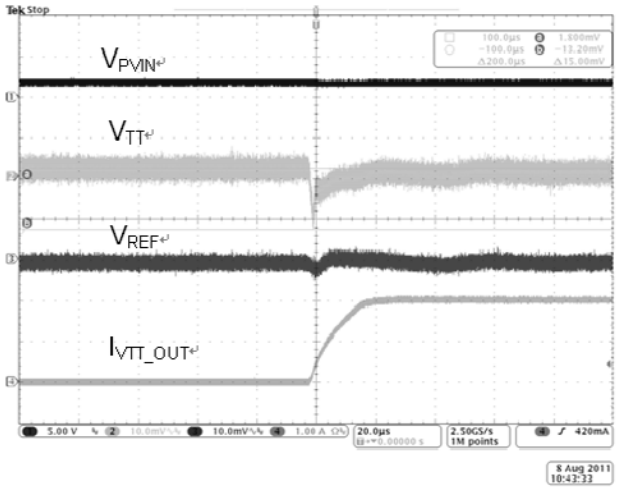


Fig.13 0.9VTT in 2A Transient respons

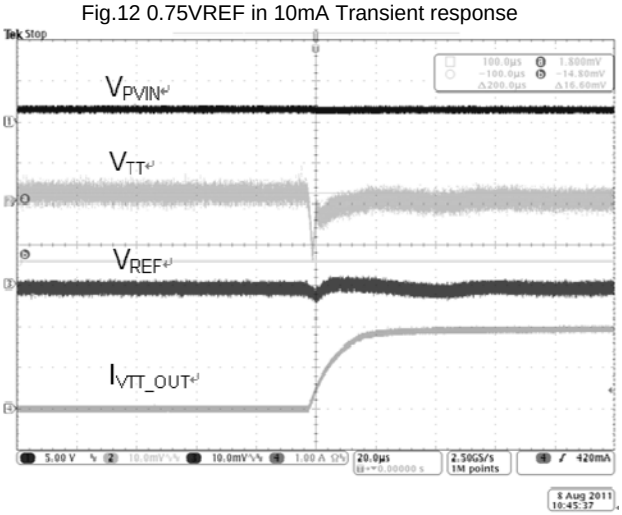
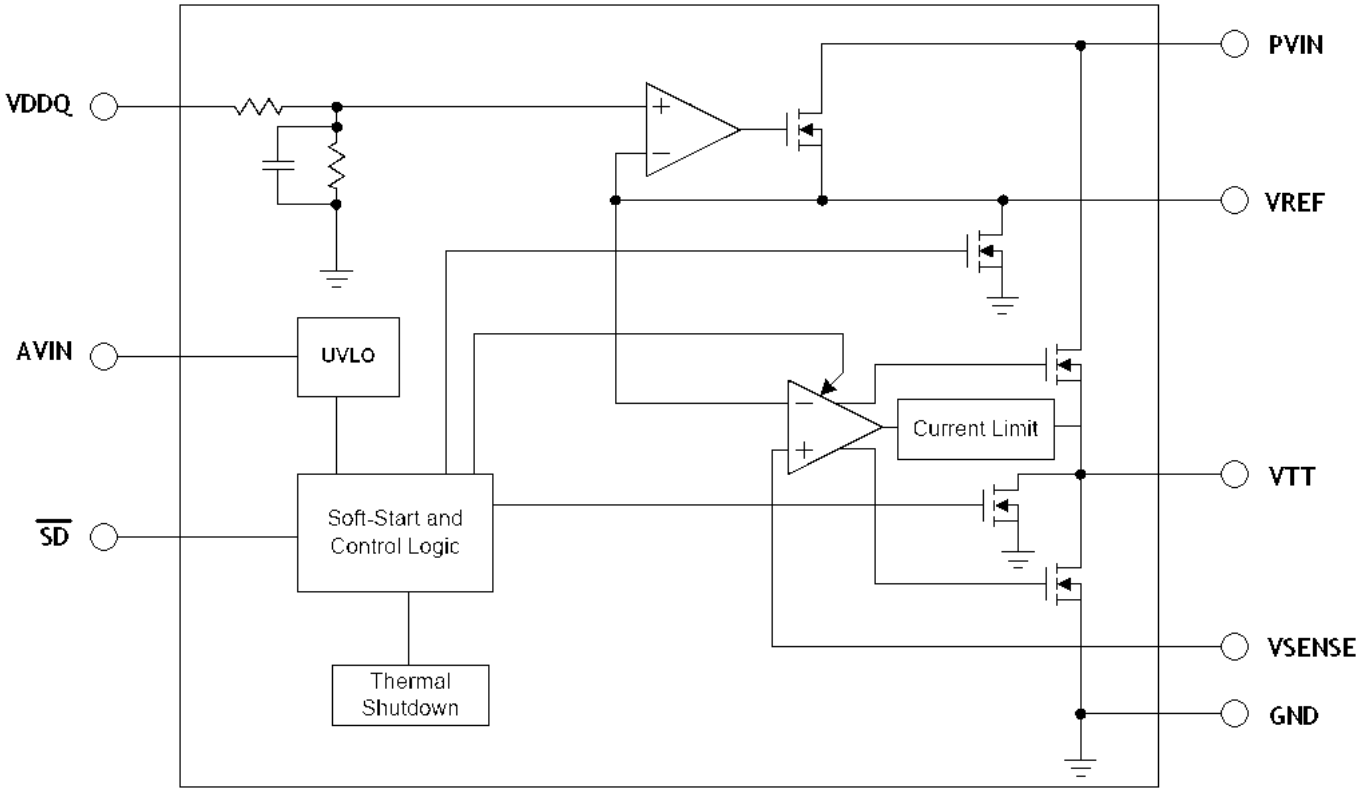


Fig.14 0.75VTT in 2A Transient respons

BLOCK DIAGRAM



AIC1386

PIN DESCRIPTION

Pin 1: GND - Ground.

Pin 2: $\overline{SD}$ - Active low shutdown pin.

Pin 3: V_{SENSE} - Sense V_{TT} to improve load regulation.

Pin 4: V_{REF} - Buffered output of internal reference voltage, equal to VDDQ/2.

Pin 5: VDDQ - Input voltage to internal reference voltage for regulating V_{TT}.

Pin 6: AVIN - Analog input voltage to supply internal control circuitry.

Pin 7: PVIN - Power input voltage to supply the rail voltage exclusively for the output stage used to create V_{TT}.

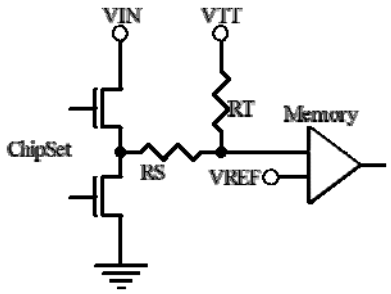
Pin 8: V_{TT} - Regulated output, equal to VDDQ/2.

Heat Sink - Recommended to Connect to GND.

APPLICATION INFORMATION

The AIC1386 linear termination regulator is designed to meet JEDEC requirements of DDR-SDRAM (DDR Ⅰ / Ⅱ / Ⅲ). The V_{TT} is able to deliver sinking and sourcing current while regulating the voltage equal to VDDQ/2. The output stage includes a sense function to maintain excellent load regulation to prevent shoot through. The power part has two distinct rails that split the internal analog circuitry from power output stage, which results in reducing internal power disspation.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is necessary to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The achievement of single parallel termination can be seen as below figure.



Between the chipset and memory are one RS series resistor and one RT termination resistor. Both RS and RT are 25 Ohms typically; they can be altered to scale the current requirements from the AIC1386.

AVIN and PVIN

AVIN and PVIN have the ability to work with separate supplies depending on the application. Higher PVIN will increase the maximum continuous output current resulting from output R_{DS-ON} limitations at voltages close to V_{TT}. Oppositely, the internal power dissipation will also increase at high PVIN. Connect AVIN and PVIN together with 2.5V is a good compromise in SSTL-2 applications. This reduces the need for bypassing two supply pins separately. For the safe operation of the system; AVIN must always exceed or equal to PVIN.

VDDQ

VDDQ is used to make internal reference voltage for regulating V_{TT}. And V_{TT} will track VDDQ/2 precisely because of internal resistor divider. For SSTL-2 application, connect VDDQ to the 2.5V rail directly at the DIMM instead of AVIN and PVIN to achieve that reference voltage tracks the DDR memory rails accurately without a voltage drop from power lines.

V_{SENSE}

The sense pin is used to improve remote load regulation. The termination resistors in most motherboards connect to V_{TT} with a long trace that will cause a significant voltage drop. The V_{SENSE} pin can improve that a lower termination voltage at one end of the bus than the other by connecting it to the middle of the bus. If a long V_{SENSE} trace is implemented close to the memory, noise pickup can be a problem in precise regulation of V_{TT}. A small 0.1µF ceramic capacitor can be used for filtering noise. V_{SENSE} pin must still tie to V_{TT} if remote load regulation is not used.

V_{REF}

V_{REF} provides the buffered output of the internal VDDQ/2 reference voltage. It can be used to support the reference voltage for the Northbridge chipset and memory. The V_{REF} remains active during the shutdown state and thermal shutdown for the Suspend to RAM functionality. A bypass capacitor, located close to the V_{REF} pin, can be used to improve performance. Ranging from 0.01µF to 0.1µF of ceramic capacitor is recommended.

V_{TT}

V_{TT} is the regulated output that is used to terminate the bus resistor, which obtains the ability of sinking and sourcing current while regulating the output accurately to VDDQ/2. The AIC1386 is designed to deliver up to ±2A peak

transient currents with excellent transient response. The output capacitor should be large enough to prevent an excessive voltage drop if a transient is expected to last above the maximum continuous current rating for a significant amount of time. AIC1386 is able to provide large transient output currents, yet it can't handle for long durations under all conditions that results from the standard packages are not able to dissipate the heat of the internal power loss. If large currents are required for longer durations, ensure that the maximum junction temperature is not exceeded.

Capacitor Selection

The input capacitor of AIC1386 is required for improved performance during large load transients to prevent the input rail from dropping. 47µF aluminum electrolytic capacitors or ceramic capacitor is recommended. If AVIN and PVIN are separated, the 47µF capacitor should be placed as close as possible to the PVIN. And AVIN can bypass a 0.1uF ceramic capacitor to prevent excessive noise.

220µF aluminum electrolytic capacitor is a recommendation for output capacitor to improve load transient response of V_{TT}. And size above 22uF ceramic output capacitor is allowed to general used for obtain small profile. The value of ESR is determined by the acceptable maximum current spike and the output voltage droops.

Thermal Dissipation

The AIC1386 has a thermal-limiting circuitry, which is designed to protect the device against overload condition. For continuous load condition, maximum rating of junction temperature must not be exceeded. It is important to pay more attention in thermal resistance. It includes junction to case, junction to ambient. The maximum power dissipation of AIC1386 depends on the thermal resistance of its case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The thermal resistance is greatly affected by the package used, the number of vias, the speed of airflow and the thickness of copper. When the IC mounting with good thermal conductivity is used, the junction temperature will be low even when large power dissipation applies. So the PCB mounting pad for GND pin of AIC1386 should provide maximum thermal conductivity to maintain low device temperature.

The power dissipation across the device is

$$P = I_{OUT} (V_{IN}-V_{OUT}).$$

The maximum power dissipation is:

$$P_{MAX} = \frac{(T_{J\text{-}max} - T_A)}{R\theta_{JA}}$$

Where $T_{J\text{-}max}$ is the maximum allowable junction temperature (125°C), and T_A is the ambient temperature suitable in application.

Low VCTNL Applications

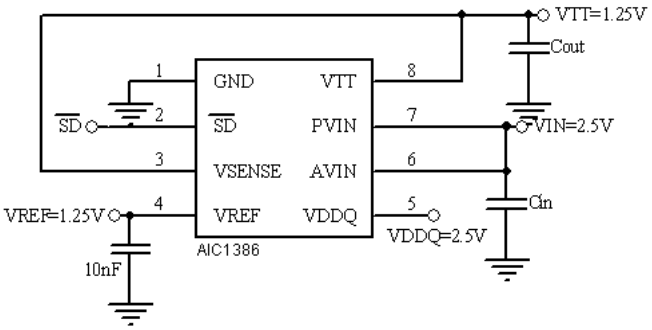
AIC1386 can be used in an application system where either a 2.5V, 3.3V or 5.0V rail is available. The VCTNL minimum input voltage requirement is 2.375V. If a 2.5V rail is used, the maximum continuous Source and Sink Current is 1.5A.

Layout Considerations

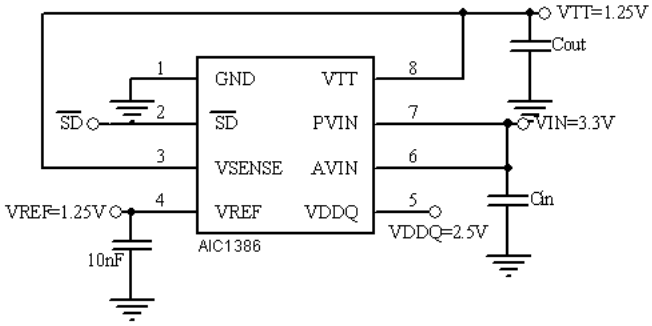
1. Minimize high current ground loops. Place the ground of the device, the input capacitor, and the output capacitor together with short and wide connection.
2. Connect the bottom-side pad (available in SOP-8 Exposed Pad) to a large ground plane. Use as much copper as possible to decrease the thermal resistance of the device.
3. A buried layer may be used as a heat spreader if the large copper around the device is not available. Use vias to lead the heat into the buried layer.
4. The input capacitor should be placed as close as possible to the PVIN pin.
5. A bypass capacitor, located close to the V_{REF} pin, can be used to improve performance. Ranging from 0.01µF to 0.1µF of ceramic capacitor is recommended.
6. If long sense traces is used, the noise of V_{SENSE} trace may occurs which from switching I/O signals. A 0.1uF ceramic capacitor connects to the V_{SENSE} pin can be used to filter high frequency signal.

APPLICATION EXAMPLES

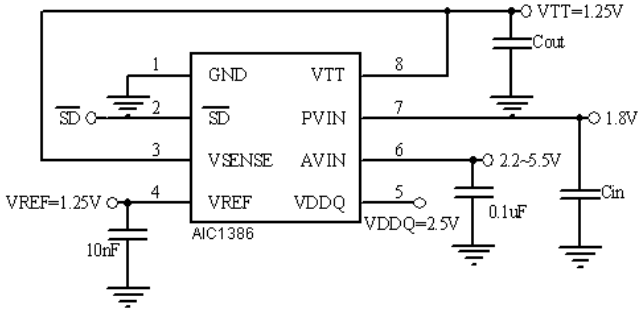
- **DDR Ⅰ Application**



All the input rails connect to 2.5V rail is recommend for the SSTL-2 termination scheme application. The circuitry completes an optimal power dissipation and component count.

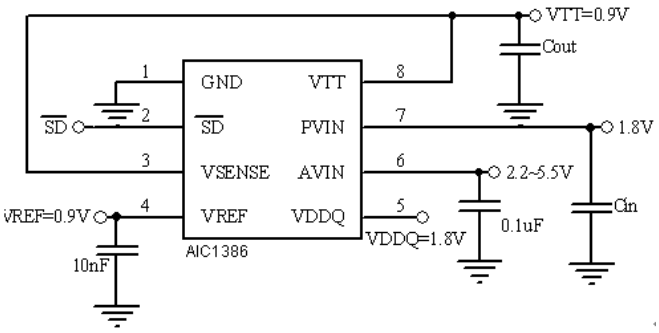


Connect the AIC1386 power rail to 3.3V to provide the maximum continuous output current if 1.8V and 2.5V rail are not available. Beware the junction temperature to exceed the maximum due to large current level. In this configuration AVIN will be limited to operation on the 3.3V or 5V rail results from PVIN can never exceed AVIN.

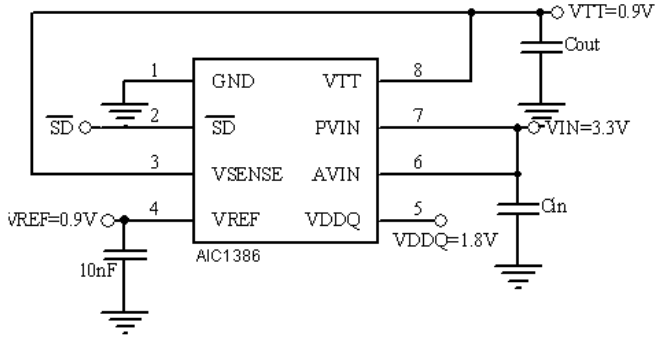


AVIN and PVIN have the ability to work with separate supplies. PVIN can be operated on a lower 1.8V rail and the AVIN can be connected to a higher rail. Although this circuitry can obtain better efficiency, but the maximum continuous current is reduced due to the lower rail voltage. Increasing the output capacitance can also help for large load transients.

- **DDR Ⅱ Application**

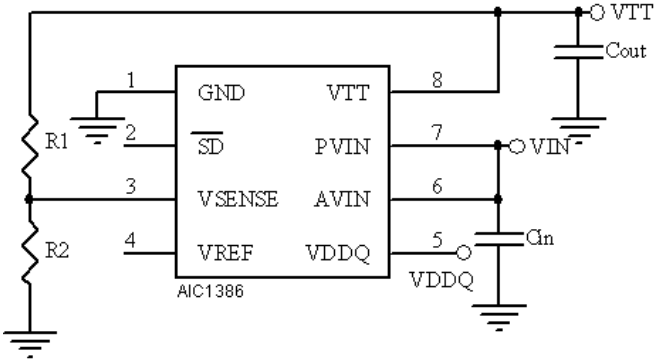


The circuit is recommended for DDR-II applications. The output stage is connected to the 1.8V rail and the AVIN pin can be connected to either a 3.3V or 5V rail.



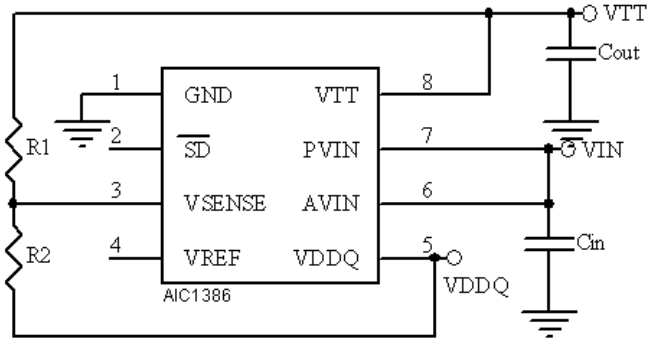
Connect the power rail to 3.3V to provide a higher continuous output current if 1.8V rail is not available. Careful with the junction temperature that may exceed the maximum due to the thermal dissipation increases with lower V_{TT} output voltages. In this configuration PVIN will be limited to operation on the 3.3V rail.

- **Level Shifting Application**



The AIC1386 is available to scale the output to any voltage required. One method is to level shift the output above the internal reference voltage of VDDQ/2 by using two resistors from the V_{TT} to the V_{SENSE}. The correct voltage at VTT is

V_{TT} = VDDQ/2 (1 + R1/R2)

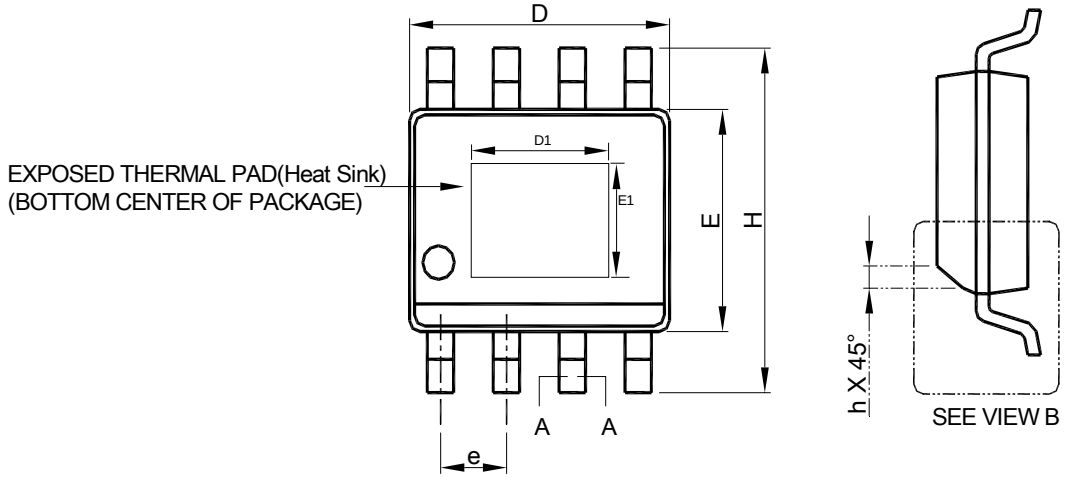


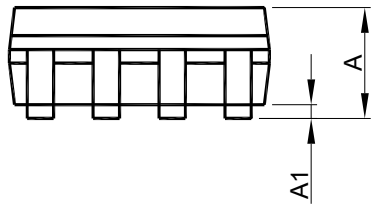
Another method is to level shift the output below the internal reference voltage of VDDQ/2 by using two resistors from the V_{SENSE} and VDDQ. The correct voltage at V_{TT} is

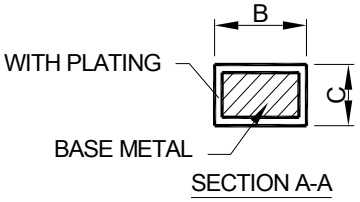
V_{TT} = VDDQ/2 (1 - R1/R2)

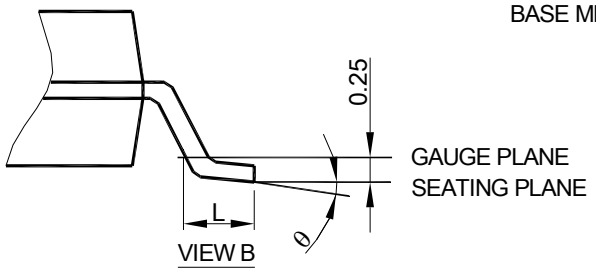
PHYSICAL DIMENSIONS (unit: mm)

- **SOP-8 Exposed Pad PACKAGE OUTLINE DRAWING**









SYMBOL	SOP-8 Exposed Pad(Heat Sink)	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.15
B	0.31	0.51
C	0.17	0.25
D	4.80	5.00
D1	1.50	3.50
E	3.80	4.00
E1	1.0	2.55
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°

Note : 1. Refer to JEDEC MS-012E.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Note: