Adjustable Precision Shunt Regulator

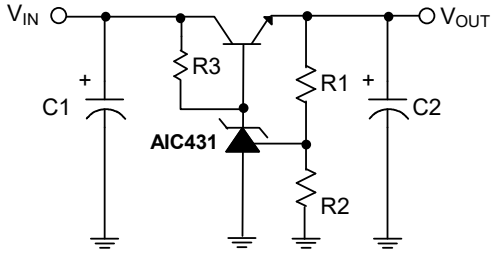
FEATURES

- Precision Reference Voltage.
  AIC431 :2.495V ±0.5%
  TL431A :2.495V ±1.0%
  TL431 :2.495V ±1.6%
- Sink Current Capability: 200mA.
- Minimum Cathode Current for Regulation: 250μA.
- Equivalent Full-Range Temperature Coefficient: 50 ppm/°C.
- Fast Turn-On Response.
- Low Dynamic Output Impedance: 0.08Ω.
- Adjustable Output Voltage.
- Low Output Noise.
- Space Saving Packages: SOT89-3, SOT23-3, and SOP-8.

APPLICATIONS

- Linear Regulators.
- Adjustable Supplies.
- Switching Power Supplies.
- Battery Operated Computers.
- Instrumentation.
- Computer Disk Drivers.

TYPICAL APPLICATION CIRCUIT



V_{OUT}=(1+R1/R2) VREF

Precision Regulator

DESCRIPTION

The AIC431, TL431A and TL431 are 3-terminal adjustable precision shunt regulators with guaranteed temperature stability over the applicable extended commercial temperature range. The output voltage may be set at any level greater than 2.495V (V_{REF}) up to 30V merely by selecting two external resistors that act as a voltage divider network. These devices have a typical output impedance of 0.08Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent improved replacements for zener diodes in many applications.

The precise ±0.5% reference voltage tolerance of the AIC431 makes it possible in many applications to avoid the use of a variable resistor, consequently saving cost and eliminating drift and reliability problems associated with it.

■ ORDERING INFORMATION

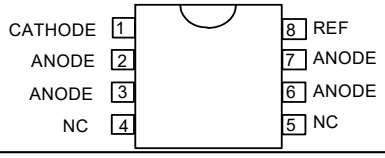
AIC431 XXXX
TL431A XXXX
TL431 XXXX

- PACKING TYPE
  TR: REEL
  TB: TUBE (for SOP-8)
  BG: BAG
- PACKAGE TYPE
  S: SOP-8
  US: SOT23-3
  UN: SOT23-3
  X: SOT89-3
- G: Green Package

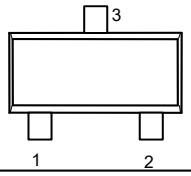
Example: AIC431GSTR
→ in SOP-8 Green Package & Taping & Reel Packing Type (GS is not available in BAG packing type.)

PIN CONFIGURATION

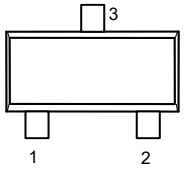
SOP-8
TOP VIEW



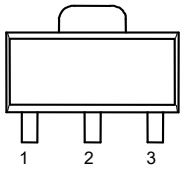
SOT23-3 (UN)
TOP VIEW
1: CATHODE
2: VREF
3: ANODE



SOT23-3 (US)
TOP VIEW
1: VREF
2: CATHODE
3: ANODE



SOT89-3
TOP VIEW
1: VREF
2: ANODE
3: CATHODE



- **SOT23-3 Marking**

Part No.	GUN
AIC431	AC1NG
TL431	AC2NG
TL431A	AC3NG

Part No.	GUS
AIC431	AC1SG
TL431	AC2SG
TL431A	AC3SG

- **SOT89-3 Marking**

Part No.	GX
AIC431	AC1BG
TL431	AC2BG
TL431A	AC3BG

ABSOLUTE MAXIMUM RATINGS

Cathode Voltage		30V
Continuous Cathode Current		-10mA ~ 250mA
Reference Input Current Range		10mA
Operating Temperature Range		–40°C to 85°C
Maximum Junction Temperature		125°C
Storage Temperature Range		–65°C to 150°C
Lead Temperature (Soldering, 10 sec)		260°C
Power Dissipation	SOT-89 Package	0.80W

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

TEST CIRCUIT

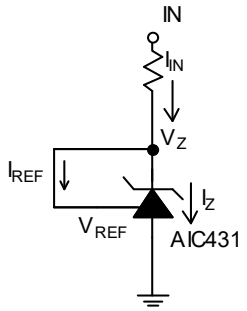
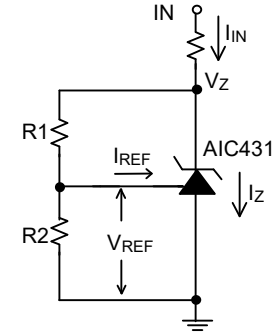


Fig. 1 Test Circuit for $V_Z=V_{REF}$



Note: $V_Z=V_{REF}(1+R1/R2)+I_{REF}xR1$

Fig. 2 Test Circuit for $V_Z>V_{REF}$

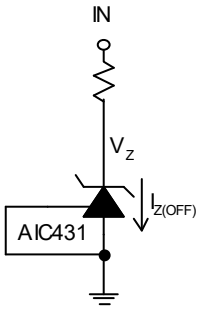


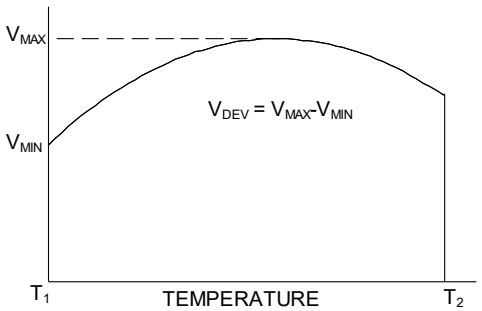
Fig. 3 Test Circuit for off-state Current

■ ELECTRICAL CHARACTERISTICS

(T_A=25°C, unless otherwise specified.) (Note 1)

PARAMETER	TEST CONDITIONS		SYMBOL	MIN.	TYP.	MAX.	UNIT
Reference Voltage	V_Z=V_{REF}, I_{IN} =10mA (Fig. 1)	AIC431	V_{REF}	2.482	2.495	2.508	V
		TL431A		2.470	2.495	2.520	
		TL431		2.455	2.495	2.535	
Deviation of Reference Input Voltage Over Temperature **(Note 2)**	V_Z = V_{REF} , I_{IN} =10mA,		V_{DEV}				mV
	T_A = 0°C~ +70°C (Fig. 1)				9.0	20	
	T_A = -40°C~ +85°C (Fig. 1)				9.0	50	
Ratio of the Change in Reference Voltage to the Change in Cathode voltage	I_Z=10mA (Fig. 2)	ΔV_Z=10V-V_{REF}	$\frac{\Delta V_{REF}}{\Delta V_Z}$		-0.5	-2.0	mV/V
		ΔV_Z=30V-10V			-0.35	-1.5	mV/V
Reference Input Current	R1 =10KΩ, R2=∞, I_{IN} =10mA (Fig. 2)		I_{REF}		0.8	3.5	μA
Deviation of Reference Input Current over Temperature	R1 =10KΩ, R2=∞, I_{IN} =10mA T_A =-40°C ~ +85°C (Fig. 2)		αI_{REF}		0.3	1.2	μA
Minimum Cathode current for Regulation	V_Z=V_{REF} (Fig. 1)		$I_{Z(MIN)}$		0.25	0.5	mA
Off-State Current	V_Z=20V, V_{REF} =0V (Fig. 3)		$I_{Z(OFF)}$		0.1	1.0	μA
Dynamic Output Impedance **(Note 3)**	V_Z=V_{REF} F<1KHz (Fig. 1)		R_Z		0.08	0.3	Ω

Note 1: Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).



Note 2: Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range.

The average temperature coefficient of the reference input voltage, αV_{REF} is defined as:

$$\Delta VREF\frac{ppm}{°C} = \frac{\pm\left[\frac{VMAX - VMIN}{VREF(at\ 25°C)}\right]10^6}{T2-T1} = \frac{\pm\left[\frac{VDEV}{VREF(at\ 25°C)}\right]}{T2-T1}$$

Where:

T_2–T_1=full temperature change.

αV_{REF} can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV}= 9.0mV, V_{REF}= 2495mV,

T_2–T_1= 70°C, slope is negative.

$$\alpha VREF = \frac{\left[\frac{9.0mV}{2495mV}\right]10^6}{70°C} = -50ppm/°C$$

Note 3: The dynamic output impedance, R_Z, is defined as:

$$R_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see Fig. 2), the dynamic output impedance of the overall circuit, is defined as:

$$rz = \frac{\Delta V}{\Delta I} \cong Rz\left[1+\frac{R1}{R2}\right]$$

TYPICAL PERFORMANCE CHARACTERISTICS

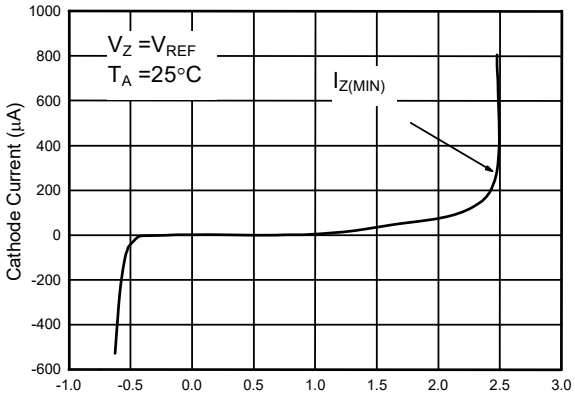


Fig. 4 Cathode Current vs. Cathode Voltage

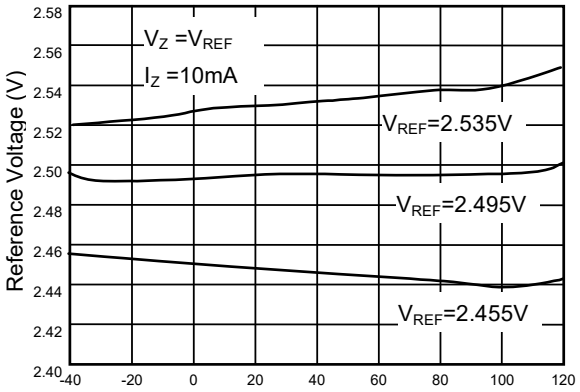


Fig. 5 Reference Voltage vs. Temperature

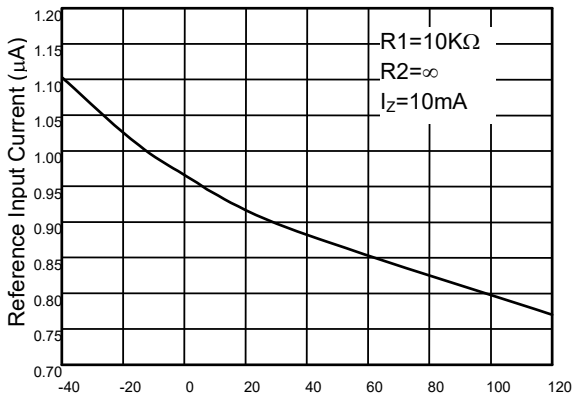


Fig. 6 Reference Input Current vs. Temperature

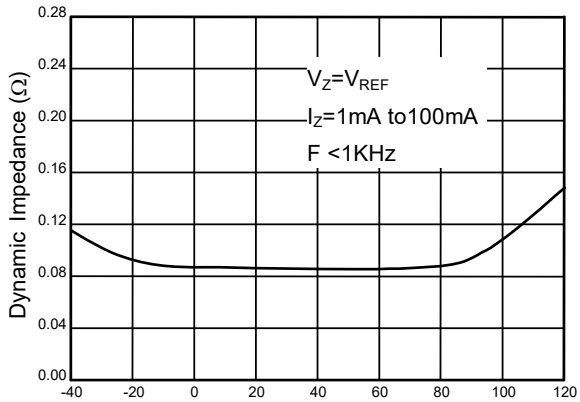


Fig. 7 Dynamic Impedance vs. Temperature

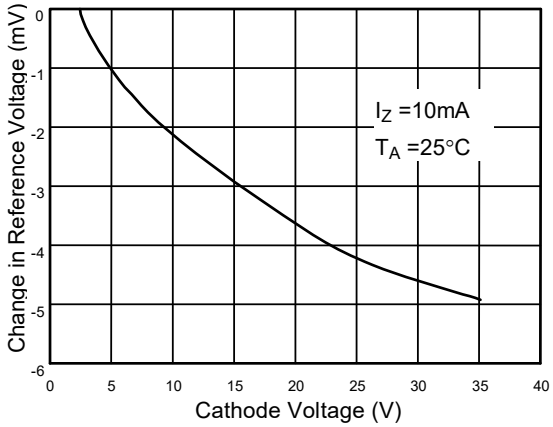


Fig. 8 Change in Reference Voltage vs. Cathode Voltage

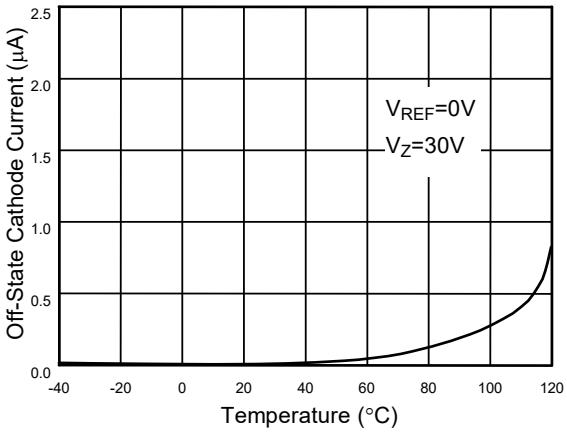


Fig. 9 Off-State Cathode Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

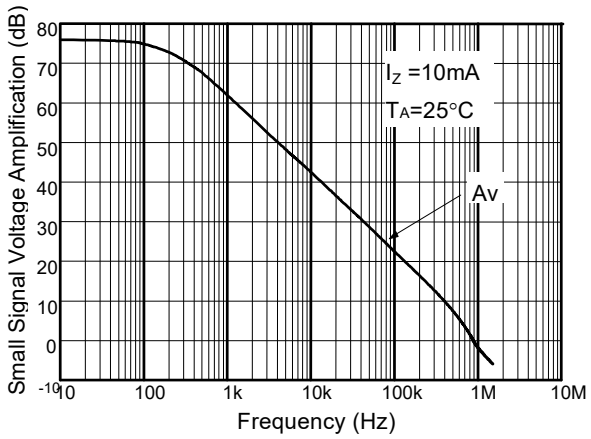


Fig. 10 Small Signal Voltage Amplification vs. Frequency

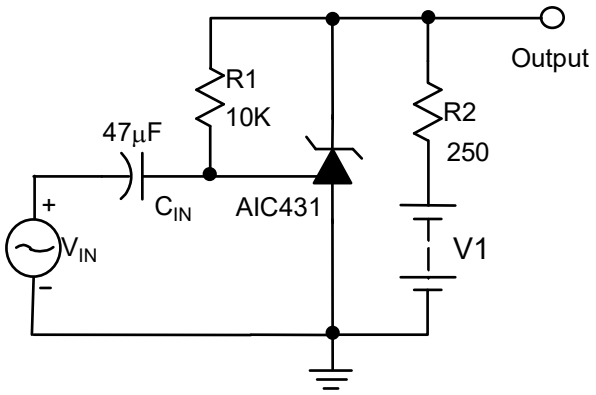


Fig. 11 Test Circuit For Frequency Response

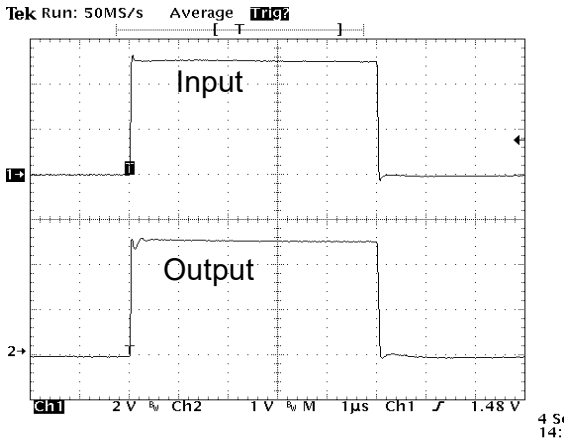


Fig. 12 Pulse Response

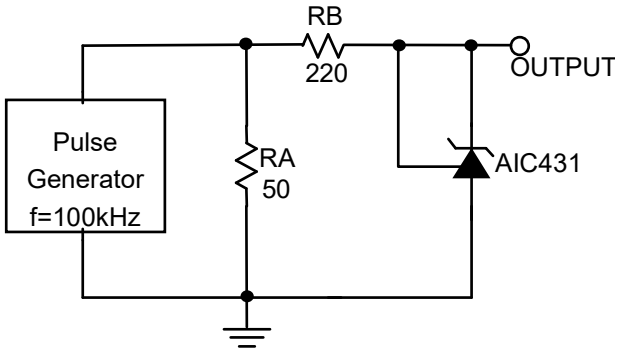


Fig. 13 Test Circuit For Pulse Response

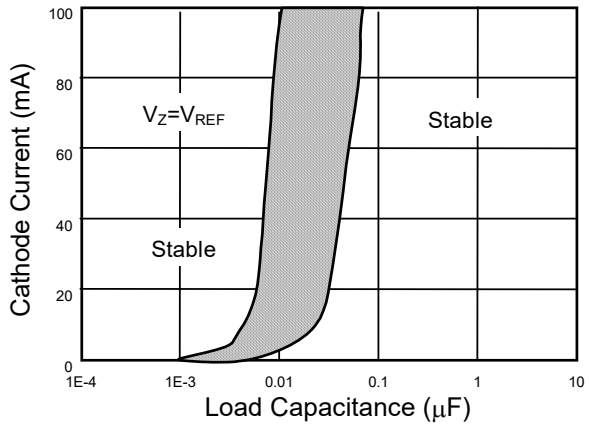


Fig. 14 Stability Boundary Conditions

The areas between the curves represent condition that may cause the device oscillate

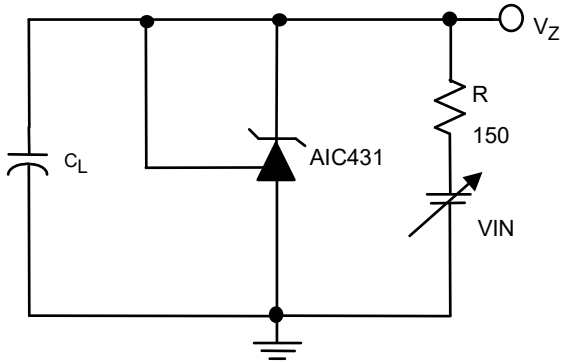


Fig. 15 Test Circuit for Stability Boundary

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

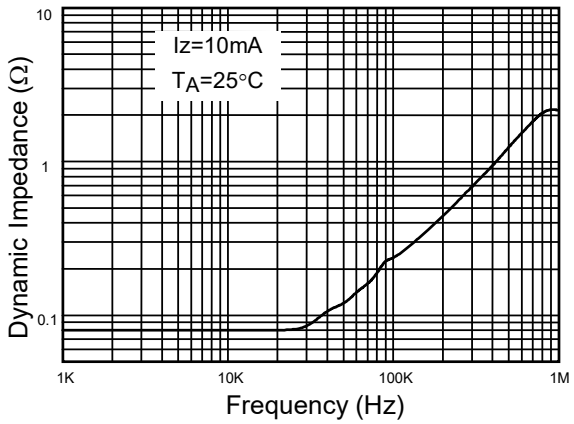


Fig. 16 Dynamic impedance vs. Frequency

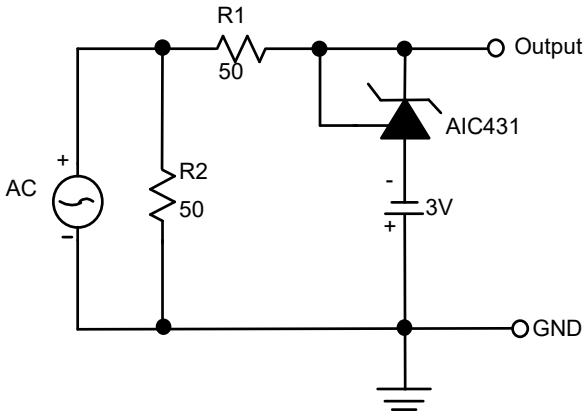
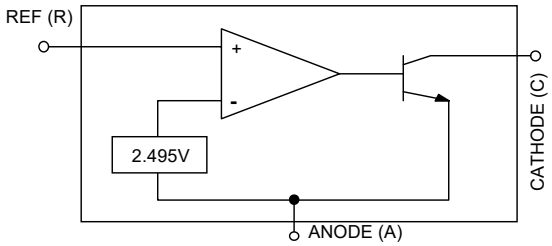
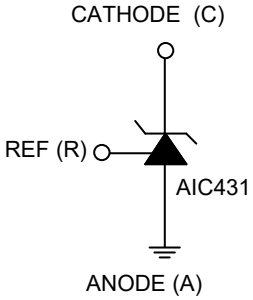


Fig. 17 Test Circuit for Dynamic Impedance

BLOCK DIAGRAM



SYMBOL



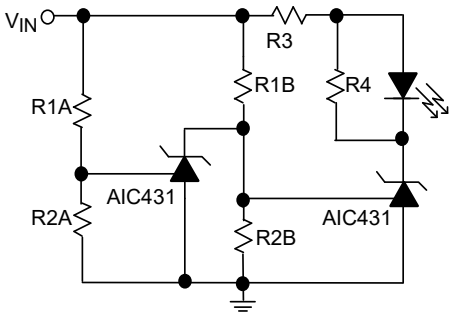
PIN DESCRIPTIONS

CATHODE Pin - Sinks current with a range from 250μA to 200mA for normal applications.

VREF Pin - Providing V_{REF}=2.495V (typ.) for adjustable output voltage.

ANODE Pin - Anode pin sources current for normal application. The current value is the same as Cathode pin.

APPLICATION EXAMPLES

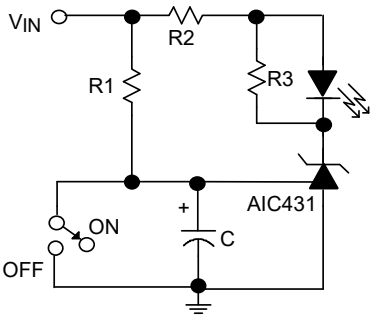


LED Turn on when Low Limit<V_{IN}< High Limit

Low Limit ≅ V_{REF} (1+R1B/R2B)

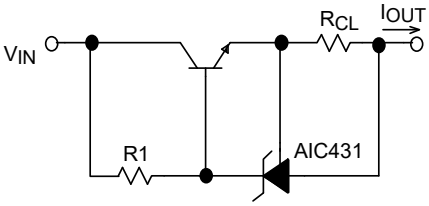
High Limit ≅ V_{REF} (1+R1A/R2A)

Fig. 18 Voltage Monitor



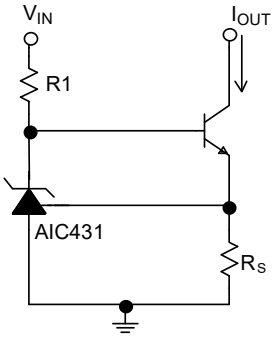
Delay=R x C x $\ell n\,(\frac{V_{IN}}{V_{IN}-V_{REF}})$

Fig. 19 Delay Timer



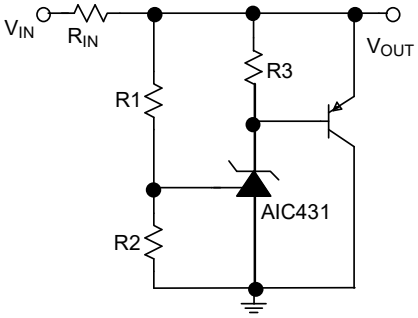
$I_{OUT}=V_{REF}/R_{CL}$

Fig. 20 Current Limiter or Current Source



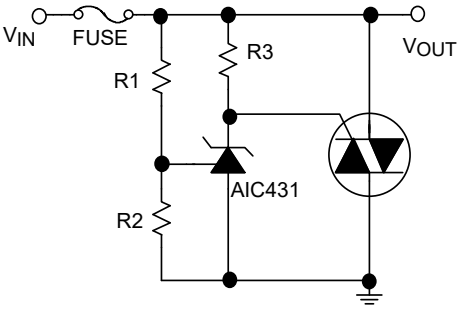
$I_{OUT}=V_{REF}/R_S$

Fig. 21 Constant-Current Sink



V_{OUT} ≅ (1+R1/R2) x V_{REF}

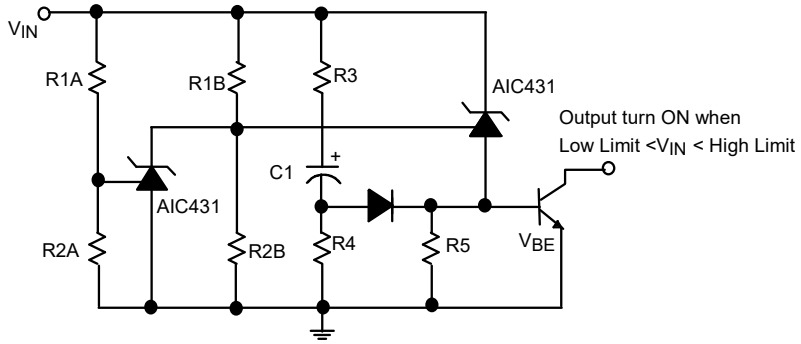
Fig 22. Higher-Current Shunt Regulator



V_{LIMIT} ≅ (1+R1/R2) x V_{REF}

Fig 23 Crow Bar

■ APPLICATION EXAMPLES (Continued)

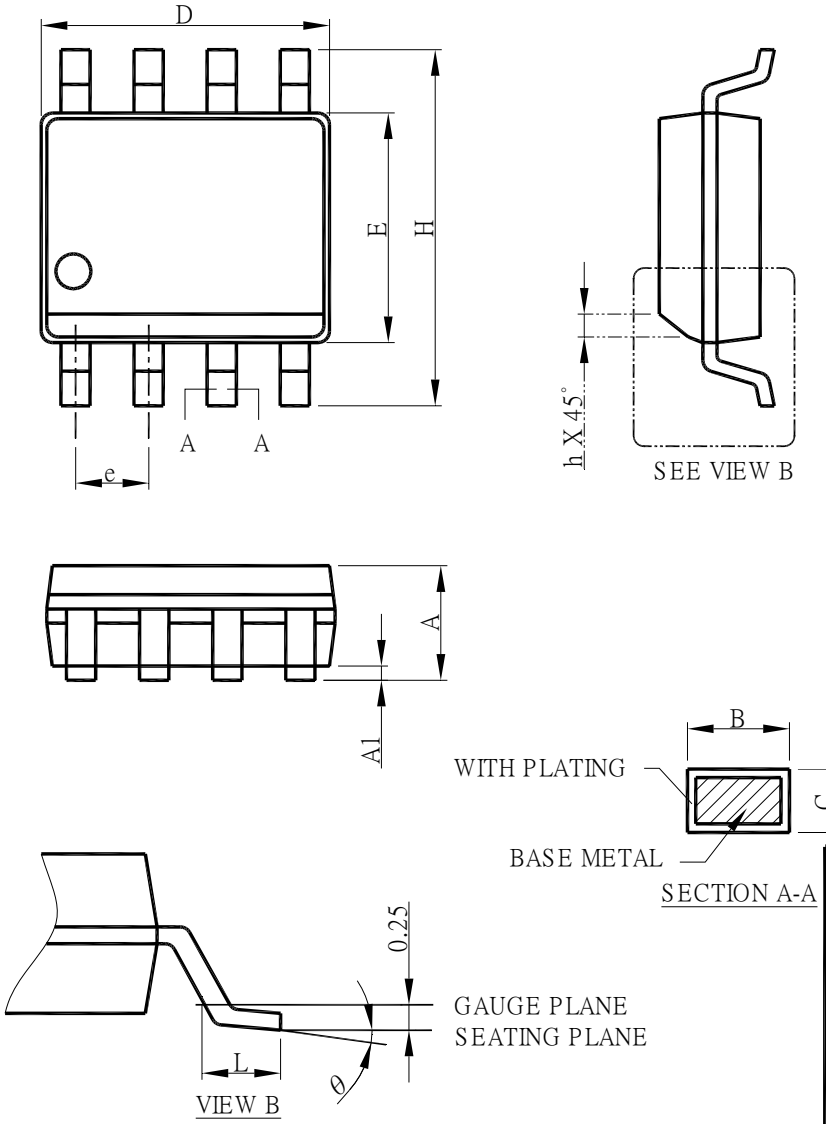


Low Limit≅ V_{REF} (1+ R1B/ R2B)+ V_{BE}
High Limit ≅ V_{REF} (1+ R1A/ R2A)

Fig 24. Over-Voltage/Under-Voltage Protection Circuit

PHYSICAL DIMENSIONS (unit: mm)

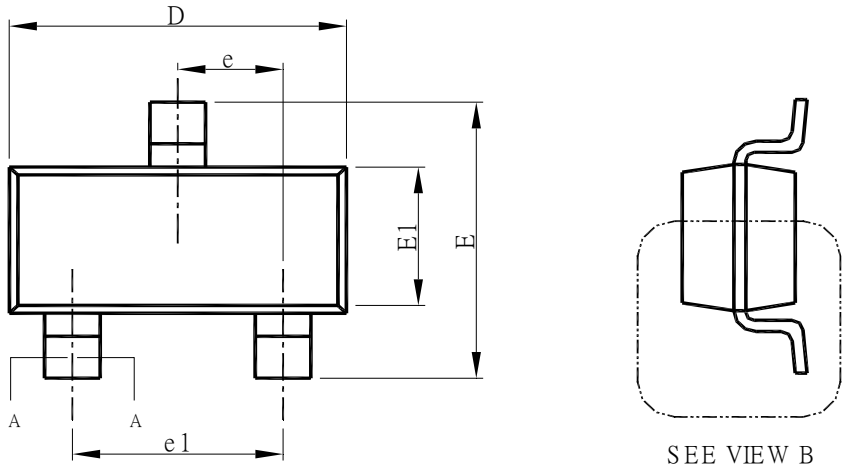
- **SOP-8**

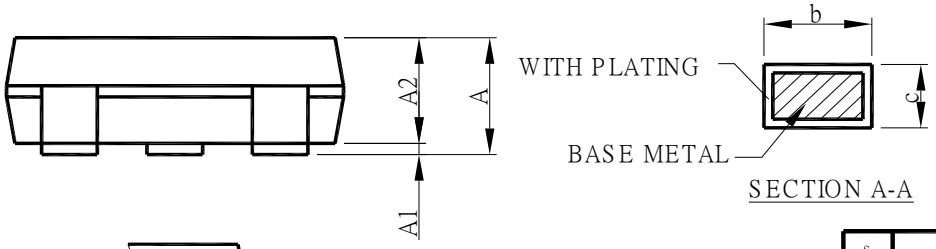


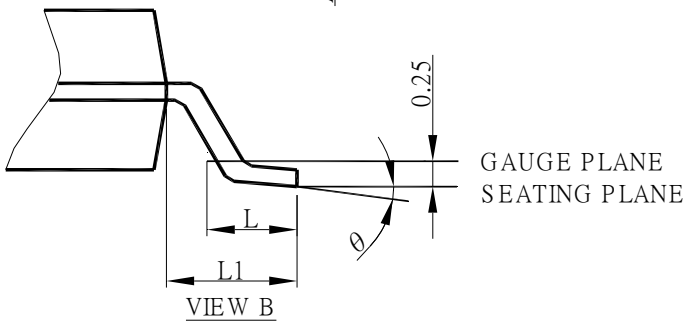
SYMBOL	SOP-8	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°

Note: 1. Refer to JEDEC MS-012AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

- **SOT23-3**



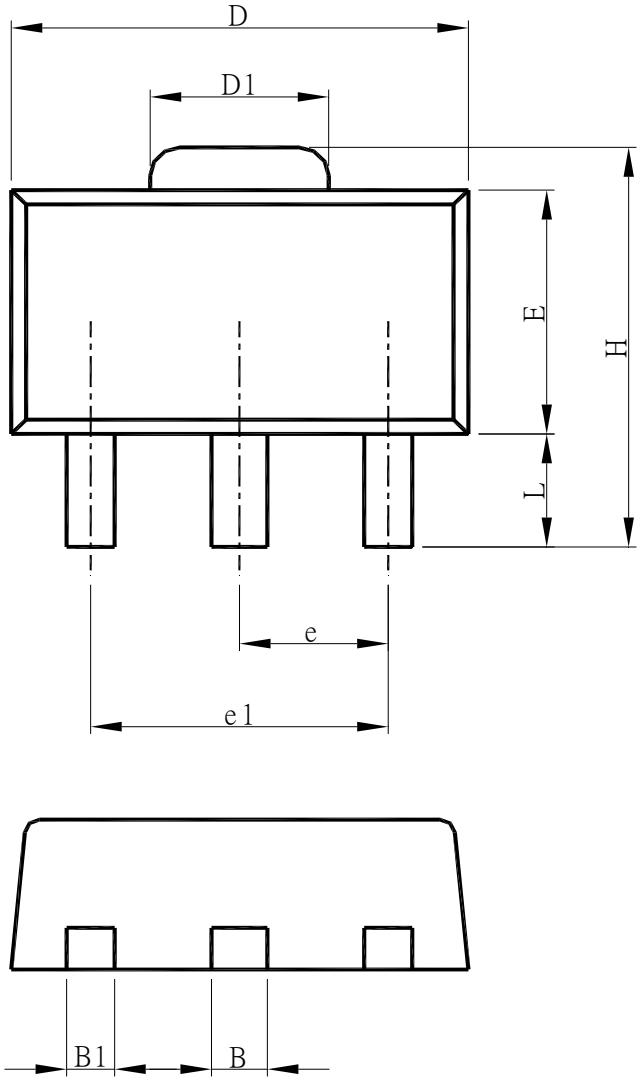




SYMBOL	SOT23-3	
	MILLIMETERS	
	MIN.	MAX.
A	0.95	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L1	0.60 REF	
θ	0°	8°

Note: 1. Refer to JEDEC MO-178.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

- **SOT89-3**



SYMBOL	SOT89-3	
	MILLIMETERS	
	MIN.	MAX.
A	1.40	1.60
B	0.44	0.56
B1	0.36	0.48
C	0.35	0.44
D	4.40	4.60
D1	1.50	1.83
E	2.29	2.60
e	1.50 BSC	
e1	3.00 BSC	
H	3.94	4.25
L	0.89	1.20

Note: 1. Refer to JEDEC TO-243AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.