

30V, 3A Wide-Input Range Step-Down Synchronous DC/DC Converter

FEATURES

- 36V Input Voltage Surge
- Wide input voltage Range: 8V~30V
- Up to 3A Output Current
- 130kHz~500kHz Adjustable Frequency
- Internal Compensation
- 32V Input OVP Protection
- Output OVP Protection
- Efficiency up to 93%
- ±2% Feedback Voltage Accuracy
- Integrated Soft Start
- Thermal Shutdown
- Constant Current Limit
- Short Circuit Hiccup Mode
- Cycle-by-Cycle Current Limit
- SOP-8 Exposed Pad

■ DESCRIPTION

AIC2933B is a wide input voltage, high efficiency step-down DC/DC converter that operates in force PWM mode with adjustable switching frequency. AIC2933B provides up to 3A output current. Switching frequency can be set by external resistor. AIC2933B internal Integrate $80m\Omega$ high side and $60m\Omega$ low side power MOSFET, which allows a high efficiency over the wider range of the load. Advanced production features include input UVLO, thermal shutdown, soft start and input and output OVP.

The AIC2933B requires a minimum number of readily available standard external components and is available in an 8-pin SOP-8 Exposed Pad.

APPLICATIONS

- Auto Electronic Equipment
- TV/Monitor
- Distributed Power Systems
- Networking Systems

■ TYPICAL APPLICATIONS CIRCUIT

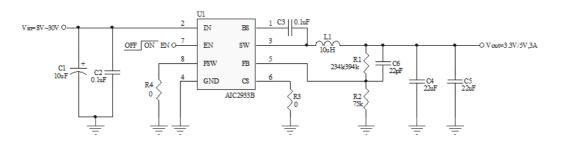


Fig. 1 Typical Application Circuit as DC/DC Converter

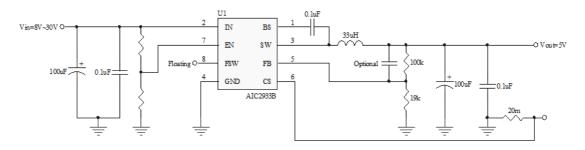


Fig. 2 Typical Application Circuit as Car Charger Converter with CC Function

Analog Integrations Corporation Si-So

Si-Soft Research Center

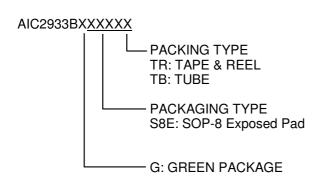
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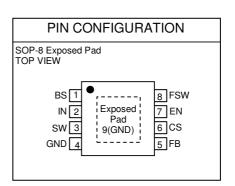
1A1, 1 Li-Hsin 1st Rd., Science Park, Hsinchu 300, Taiwan, R.O.C.

FAX: 886-3-5772510



ORDERING INFORMATION





Example:

AIC2933BGS8ETR

→ Green SOP-8 Exposed Pad Package and TAPE & REEL Packing Type

Marking

| Part No. | Marking | |
|--------------|---------|--|
| AIC2933BGS8E | T3331 | |

■ ABSOLUTE MAXIMUM RATINS

| IN Pin, SW Pin and EN Pin Voltage | | 0.3V to 36V |
|--|-------------------|---------------|
| BS to SW Voltage | | 0.3V to 6V |
| Pin Voltage for all other Pins | | 0.3V to 6V |
| Junction Temperature (Note 2) | | 40°C to 150°C |
| Storage Temperature Range | | 65°C to 150°C |
| Thermal Resistance Junction to Case | SOP-8 Exposed Pad | 46°C/W |
| Thermal Resistance Junction to Ambient | SOP-8 Exposed Pad | 60°C/W |
| Package Power Dissipation | SOP-8 Exposed Pad | 2W |
| | | |

(Assume no Ambient Airflow)

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.



ELECTRICAL CHARACTERISTICS

(V_{IN}=24V, V_{EN} =5V, T_A=25°C, unless otherwise specified.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|----------------------|----------------------------------|------|-----|-----|-------|
| Input Voltage Range | V _{IN} | | 8 | | 30 | V |
| Input Voltage Surge | V_{IN} | | | | 36 | V |
| Under Voltage Lockout | V_{UVLO} | V _{IN} rising | | 7.2 | | V |
| UVLO Hysteresis | V _{UVLO HY} | | | 0.6 | | V |
| Quiescent Supply Current | I _{CCQ} | No Load, V _{FB} > 0.83V | | 1 | | mA |
| Standby Supply Current | I _{STBY} | V _{OUT} =5V, No Load | | 10 | 15 | mA |
| Feedback Threshold Voltage | V_{FBTH} | | 784 | 800 | 816 | mV |
| FB Pin Input Current | I _{FB} | | -50 | | 50 | nA |
| Input OVP Voltage | V _{INOVP} | | 31.5 | | | ٧ |
| Output OVP Voltage | V _{OUTOVP} | | | 10 | 20 | % |
| Soft Start Time | T _{SST} | | | 4 | | ms |
| CS Current Limit Voltage | V _{LIM CS} | | | 64 | | mV |
| SW Leakage | I _{SW LEAK} | | | | 10 | μΑ |
| Maximum Duty Cycle | D _{DUTY} | F _S =300kHz | | | 90 | % |
| | | R_{FSW} =300k Ω | | 310 | | |
| Switching Frequency | Fs | FSW pin floating | | 130 | | kHz |
| | | FSW pin short to GND | | 500 | | |
| Switch On-Resistance (H side) | R _{ON HS} | By Design | | 80 | | mΩ |
| Switch On-Resistance (L side) | R _{ON LS} | By Design | | 60 | | mΩ |
| Short Circuit Frequency | F _{SC} | V _{FB} =0V | | 35 | | kHz |
| Minimum Turn-on Time | T _{ON MIN} | | | 200 | | ns |
| EN High Level Input Voltage | V _{EN H} | | 1.5 | | | V |
| EN Low Level Input Voltage | V _{EN L} | | | | 0.3 | ٧ |
| Thermal Shutdown Threshold (Note 3) | T_{SDN} | | | 155 | | ç |
| Thermal Shutdown Hysteresis (Note 3) | T _{SDN HY} | | | 20 | | Ç |

- Note 1: Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).
- Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D (MAX)} = (T_{J(MAX)} T_A)/\theta_{JA}$.
- Note 3: Thermal shutdown threshold and hysteresis are guaranteed by design.



TYPICAL PERFORMANCE CHARACTERISTICS

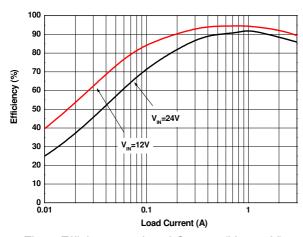


Fig. 3 Efficiency vs. Load Current (V_{OUT}=5V)

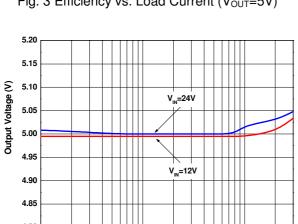


Fig. 5 Output Voltage vs. Load Current (V_{OUT} =5V)

Load Current (A)

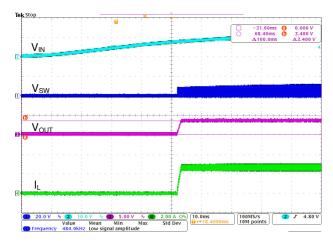


Fig. 7 V_{IN} Power On (V_{IN} =12V, V_{OUT} =3.3V, I_{OUT} =3A)

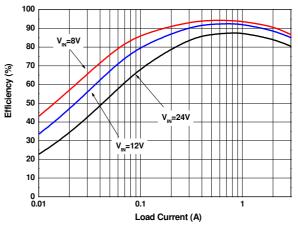


Fig. 4 Efficiency vs. Load Current (V_{OUT}=3.3V)

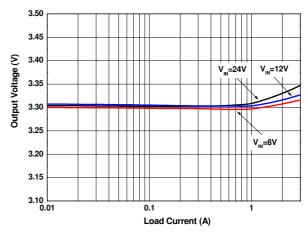


Fig. 6 Output Voltage vs. Load Current (V_{OUT}=3.3V)

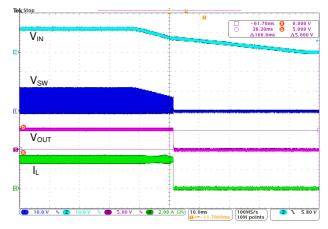
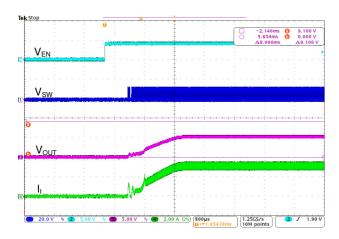
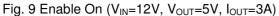


Fig. 8 V_{IN} Power Off (V_{IN} =12V, V_{OUT} =5V, I_{OUT} =3A)



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)





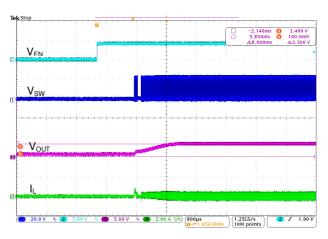


Fig. 10 Enable On (V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=0A)

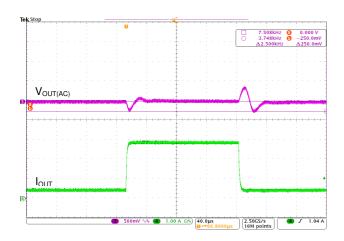


Fig. 11 Load Transient (V_{IN}=12V, V_{OUT}=3.3V, I_O=0.3-2.7A)

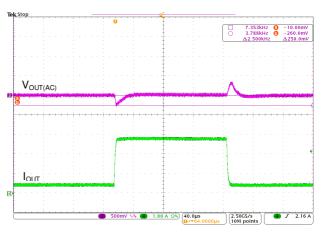


Fig. 12 Load Transient (V_{IN} =24V, V_{OUT} =5V, I_O =0.3-2.7A)

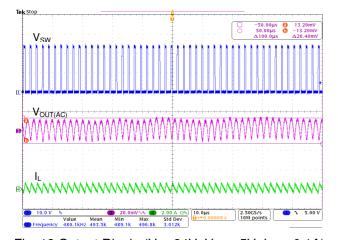


Fig. 13 Output Ripple (V_{IN} =24V, V_{OUT} =5V, I_{OUT} =0.1A)

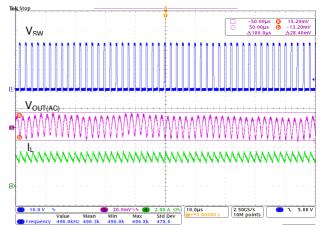
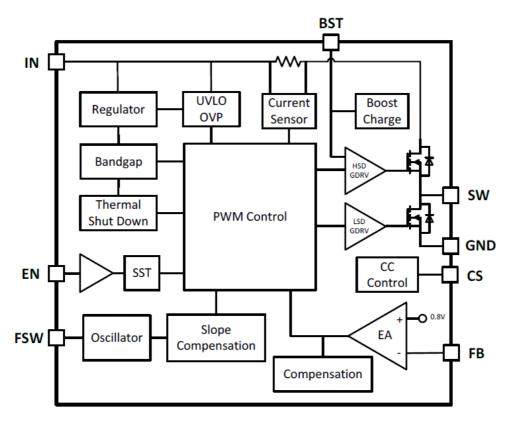


Fig. 14 Output Ripple (V_{IN}=24V, V_{OUT}=5V, I_{OUT}=3A)



BLOCK DIAGRAM



Functional Block Diagram

■ PIN DESCRIPTIONS

| Pin No. | Pin Name | Pin Function | |
|---------|----------------------|--|--|
| 1 BS | | High side Gate Driver bias pin. Provide supply to high-side LDMOS Gate Driver. | |
| | | Connect a 100nF capacitor between BS and SW. | |
| 2 | IN | Power Input Pin. | |
| 3 | SW | Switch Pin. Connect to External Inductor. | |
| 4 | GND | Power Ground. | |
| 5 | FB | Output Voltage Feedback Pin. | |
| 6 | CS | Output Current Sense Pin for Constant Current Limit. | |
| 7 | EN | Enable Pin. | |
| 8 | FSW | Switching Frequency set pin. Short to GND: F _S =500kHz. | |
| 9 | GND (Exposed Pad) | Ground (Exposed PAD). | |



APPLICATION INFORMATION

AIC2933B is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows: A switching cycle starts when the rising edge of the oscillator clock output causes the High- Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off.

At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using BS as the positive rail. This pin is charged to VSW + 5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.8V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase and the output voltage be regulated.

Output Voltage Setting

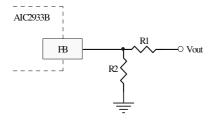


Fig. 15 Output Voltage Setting

Figure 15 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_1 and R_2 based on the output voltage. Adding a capacitor in parallel with R1 helps the system stability. Typically, use $R_2 \approx 75 \mathrm{k}\Omega$ and determine R_1 from the following equation:

$$R_{1} = R_{2} \times \left(\frac{V_{OUT}}{0.8V} - 1 \right)$$

For DC/DC application with only ceramic output capacitors (two paralleling 22 μ F capacitors or one 47 μ F capacitor are recommended), a 22 μ F feedforward capacitor paralleling with R1 (R1 is recommended larger than 200 μ C resistance) is recommended for stability and better load transient performance.

Over Voltage Protection

The thresholds of input OVP circuit include are minimum 31.5V. Once the input voltage is higher than the threshold, the high-side MOSFET is turned off. When the input voltage drops lower than the threshold, the high-side MOSFET will be enabled again.

Thermal Shutdown

The AIC2933B disables switching when its junction temperature exceeds 155 °C and resumes when the temperature has dropped by 20 °C.

Setting the Switching Frequency

The oscillator normally switches at 130kHz~500kHz, which is set by FSW resistance as Table 1.

Table 1 Switching Frequency vs. R_{FSW}

| R _{FSW} | Frequency (typ.) |
|----------------------|------------------|
| Floating | 130kHz |
| $R_{FSW}=300k\Omega$ | 310kHz |
| $R_{FSW}=250k\Omega$ | 350kHz |
| $R_{FSW}=200k\Omega$ | 410kHz |
| Short to GND | 500kHz |



Constant Current Limit Setting

A2933B has output constant current limit function. The constant current value is set by a resistor R_{CS} connected between the CS pin and GND. The CC output current is calculated by $I_{\text{LIM}}{=}64\text{mV/R}_{\text{CS}}.$ If there is no constant current limit requirement, CS could be connected to GND directly and internal cycle-bycycle peak current limit function is active with over current condition.

Setting the Cable Compensation

AIC2933B provides programmable cable voltage drop compensation using the impedance at the FB pin to compensate voltage drop across the charger's output cable if R_{CS} resistor is used between CS pin and GND. The cable compensation voltage can be expressed as: $V_{comp} = I_{load} \times 10^{-6} \times R_{FB1}$. By adjusting the value of R_{FB1} , the cable compensation voltage can be programmed.

EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on SW node when high-side MOSFET is turned on/off, this spike voltage on SW may impact on EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One is to place an RC snubber

between SW and GND and make them as close as possible to the high-side MOSFET's source and low-side MOSFET's drain. Another method is to add a resistor in series with the bootstrap capacitor C₃. But this method will decrease the driving capability to the high-side MOSFET. It is strongly recommended to reserve the RC snubber during PCB layout for EMI improvement. Moreover, reducing the PHASE trace area and keeping the main power in a small loop will be helpful on EMI performance.

PC Board Layout Guidance

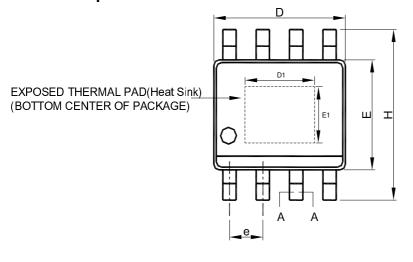
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

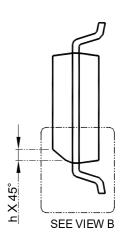
- Arrange the power components to reduce the AC loop size consisting of C_{IN}, IN pin, SW pin.
- 2. Place input decoupling ceramic capacitor C_{IN} as close to IN pin as possible. C_{IN} is connected power GND short and wide path or with vias.
- Return FB to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
- 4. Use copper plane for power GND for best heat dissipation and noise immunity.
- 5. Place feedback resistor close to FB pin.
- Use short trace connecting BS-C_{BS}-SW loop.

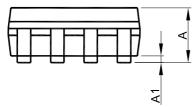


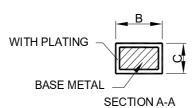
PHYSICAL DIMENSIONS

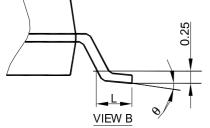
SOP-8 Exposed Pad











GAUGE PLANE SEATING PLANE

Note: 1. Refer to JEDEC MS-012E.

- 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
- 3. Dimension "E" does not include inter-lead flash or protrusions.
- 4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

| S Y | SOP-8 Exposed Pad | | |
|--------|-------------------|------|--|
| M B | MILLIMETERS | | |
| O L | MIN. | MAX. | |
| А | 1.35 | 1.75 | |
| A1 | 0.00 | 0.15 | |
| В | 0.31 | 0.51 | |
| С | 0.17 | 0.25 | |
| D | 4.80 | 5.00 | |
| D1 | 1.50 | 3.50 | |
| Е | 3.80 | 4.00 | |
| E1 | 1.0 | 2.55 | |
| е | 1.27 BSC | | |
| Н | 5.80 | 6.20 | |
| h | 0.25 | 0.50 | |
| L | 0.40 | 1.27 | |
| θ | 0° | 8° | |

Note:

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